27.7 SCI Control Registers

These registers are accessible in 8-, 16-, and 32-bit reads or writes. The SCI is controlled and accessed through the registers listed in Table 27-3. Among the features that can be programmed are the SCI communication and timing modes, baud rate value, frame format, DMA requests, and interrupt configuration.

Table 27-3. SCI Control Registers Summary

Offset	Acronym	Register Description	Section
00	SCIGCR0	SCI Global Control Register 0	Section 27.7.1
04h	SCIGCR1	SCI Global Control Register 1	Section 27.7.2
0Ch	SCISETINT	SCI Set Interrupt Register	Section 27.7.3
10h	SCICLEARINT	SCI Clear Interrupt Register	Section 27.7.4
14h	SCISETINTLVL	SCI Set Interrupt Level Register	Section 27.7.5
18h	SCICLEARINTLVL	SCI Clear Interrupt Level Register	Section 27.7.6
1Ch	SCIFLR	SCI Flags Register	Section 27.7.7
20h	SCIINTVECT0	SCI Interrupt Vector Offset 0	Section 27.7.8
24h	SCIINTVECT1	SCI Interrupt Vector Offset 1	Section 27.7.9
28h	SCIFORMAT	SCI Format Control Register	Section 27.7.10
2Ch	BRS	Baud Rate Selection Register	Section 27.7.11
30h	SCIED	Receiver Emulation Data Buffer	Section 27.7.12.1
34h	SCIRD	Receiver Data Buffer	Section 27.7.12.2
38h	SCITD	Transmit Data Buffer	Section 27.7.12.3
3Ch	SCIPIO0	SCI Pin I/O Control Register 0	Section 27.7.13
40h	SCIPIO1	SCI Pin I/O Control Register 1	Section 27.7.14
44h	SCIPIO2	SCI Pin I/O Control Register 2	Section 27.7.15
48h	SCIPIO3	SCI Pin I/O Control Register 3	Section 27.7.16
4Ch	SCIPIO4	SCI Pin I/O Control Register 4	Section 27.7.17
50h	SCIPIO5	SCI Pin I/O Control Register 5	Section 27.7.18
54h	SCIPIO6	SCI Pin I/O Control Register 6	Section 27.7.19
58h	SCIPIO7	SCI Pin I/O Control Register 7	Section 27.7.20
5Ch	SCIPIO8	SCI Pin I/O Control Register 8	Section 27.7.21
90h	IODFTCTRL	Input/Output Error Enable Register	Section 27.7.22

27.7.1 SCI Global Control Register 0 (SCIGCR0)

The SCIGCR0 register defines the module reset. Figure 27-8 and Table 27-4 illustrate this register.

Figure 27-8. SCI Global Control Register 0 (SCIGCR0) [offset = 00]

31	16
Reserved	
R-0	

15	1	0
Reserved		RESET
R-0		RWP-0

LEGEND: R/W = Read/Write; R = Read only; RWP = Read/Write in privileged mode only; -*n* = value after reset

Table 27-4. SCI Global Control Register 0 (SCIGCR0) Fied Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Read returns 0. Writes have no effect.
0	RESET		This bit resets the SCI module.
		0	SCI module is in reset.
		1	SCI module is out of reset.
			Note: Read/Write in privileged mode only.

27.7.2 SCI Global Control Register 1 (SCIGCR1)

The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI. Figure 27-9 and Table 27-5 illustrate this register.

Figure 27-9. SCI Global Control Register 1 (SCIGCR1) [offset = 04h]

31						26	25	24
Reserved							TXENA	RXENA
R-0							R/W-0	R/W-0
23						18	17	16
Reserved							CONT	LOOP BACK
R-0							R/W-0	R/W-0
15						10	9	8
Reserved							POWERDOWN	SLEEP
R-0							R/WP-0	R/W-0
7	6	5	4	3	2		1	0
SW nRST	Reserved	CLOCK	STOP	PARITY	PARITY ENA		TIMING MODE	COMM MODE
R/W-0	R-0	R/W-0	R/WC-0	R/WC-0	R/W-0		R/WC-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; WC = Write in sci-compatible mode only; -*n* = value after reset

NOTE: The SCIGCR1 Control Register Bits should not be changed during Frame Transmission or Reception..

Table 27-5. SCI Global Control Register 1 (SCIGCR1) Field Descriptions

Bit	Field	Value	Description
31-26	Reserved	0	Read returns 0. Writes have no effect.
25	TXENA		Transmit enable. Data is transferred from SCITD to the SCITXSHF shift out register only when the TXENA bit is set.
		0	Disable transfers from SCITD to SCITXSHF.
		1	Enable SCI to transfer data from SCITD to SCITXSHF.
			Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not transmitted. If TXENA is cleared while transmission is ongoing, the data previously written to SCITD is sent.
24	RXENA		Receive enable. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD.
		0	The receiver will not transfer data from the shift buffer to the receive buffe.
		1	The receiver will transfer data from the shift buffer to the receive buffer.
			Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags (see Table 27-4) from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA.
			Note: If RXENA is cleared before a frame is completely received, the data from the frame is not transferred into the receive buffer.
			Note: If RXENA is set before a frame is completely received, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flags correctly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame.
23-18	Reserved	0	Read returns 0. Writes have no effect.
17	CONT		Continue on suspend. This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI operates when the program is suspended. The
		0	When debug mode is entered, the SCI state machine is frozen. Transmissions are halted and resume when debug mode is exited.
		1	When debug mode is entered, the SCI continues to operate until the current transmit and receive functions are complete.

Table 27-5. SCI Global Control Register 1 (SCIGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
16	LOOP BACK		Loopback bit. The self-checking option for the SCI can be selected with this bit. If the SCITX and SCIRX pins are configured with SCI functionality, then the SCITX pin is internally connected to the SCIRX pin. Externally, during loop back operation, the SCITX pin outputs a high value and the SCIRX pin is in a high-impedance state. If this bit value is changed while the SCI is transmitting or receiving data, errors may result.
		0	Loop back mode is disabled.
		1	Loop back mode is enabled.
15-10	Reserved	0	Read returns 0. Writes have no effect.
9	POWERDOWN		Power down. When the POWERDOWN bit is set, the SCI attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wake-up interrupt is enabled, then the SCI immediately asserts an error interrupt to prevent low-power mode from being entered. Only Privilege mode writes allowed.
		0	Normal operation.
		1	Low-power mode is enabled.
8	SLEEP		SCI sleep. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode.
		0	Sleep mode is disabled.
		1	Sleep mode is enabled.
			Note: The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags (see Table 27-4) are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition.
			Note: The SLEEP bit is not automatically cleared when an address byte is detected.
			See Section 27.6 for more information on using the SLEEP bit for multiprocessor communication.
7	SWnRST		Software reset (active low). This bit is effective in LIN and SCI modes.
		0	The SCI is in its reset state; no data will be transmitted or received. Writing a 0 to this bit initializes the SCI state machines and operating flags as defined in Table 27-11 and Table 27-12. All affected logic is held in the reset state until a 1 is written to this bit.
		1	The SCI is in its ready state; transmission and reception can be done. After this bit is set to 1, the configuration of the module should not change.
			Note: The SCI should only be configured while SWnRESET = 0.
6	Reserved	0	Read returns 0. Writes have no effect.
5	CLOCK		SCI internal clock enable. The CLOCK bit determines the source of the module clock on the SCICLK pin.
		0	The external SCICLK is the clock source.
		1	The internal SCICLK is the clock source.
			Note: If an external clock is selected, then the internal baud rate generator and baud rate registers are bypassed. The maximum frequency allowed for an externally sourced SCI clock is VCLK/16.
4	STOP		SCI number of stop bits per frame.
		0	One stop bit is used.
		1	Two stop bits are used.
			Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit (if STOP = 1) to begin checking for an idle period.

Table 27-5. SCI Global Control Register 1 (SCIGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
3	PARITY		SCI parity odd/even selection. If the PARITY ENA bit is set, PARITY designates odd or even parity.
		0	Odd parity is used.
		1	Even parity is used.
			The parity bit is calculated based on the data bits in each frame and the address bit (in address-bit mode). The start and stop fields in the frame are not included in the parity calculation.
			For odd parity, the SCI transmits and expects to receive a value in the parity bit that makes odd the total number of bits in the frame with the value of 1.
			For even parity, the SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.
2	PARITY ENA		Parity enable. This bit enables or disables the parity function.
		0	Parity is disabled; no parity bit is generated during transmission or is expected during reception.
		1	Parity is enabled. A parity bit is generated during transmission and is expected during reception.
1	TIMING MODE		SCI timing mode bit.
		0	Synchronous timing is used.
		1	Asynchronous timing is used.
0	COMM MODE		SCI communication mode bit.
		0	Idle-line mode is used.
		1	Address-bit mode is used.

27.7.3 SCI Set Interrupt Register (SCISETINT)

Figure 27-10 and Table 27-6 illustrate this register. SCISETINT register is used to enable the required interrupts supported by the module.

Figure 27-10. SCI Set Interrupt Register (SCISETINT) [offset = 0Ch]

31	27	26	25	24
Reserved		SET FE INT	SET OE INT	SET PE INT
R-0		R/W-0	R/W-0	R/W-0
23	19	18	17	16
Reserved		SET RX DMA ALL	SET RX DMA	SET TX DMA
R-0		R/WC-0	R/W-0	R/W-0
15		10	9	8
Reserved			SET RX INT	SET TX INT
R-0			R/W-0	R/W-0
7		2	1	0
Reserved			SETWAKEUPINT	SET BRKDT INT
R-0			R/W-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; WC = Write in sci-compatible mode only; *-n* = value after reset

Table 27-6. SCI Set Interrupt Register (SCISETINT) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Read returns 0. Writes have no effect.
26	SET FE INT		Set framing-error interrupt. Setting this bit enables the SCI module to generate an interrupt when a framing error occurs.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.
25	SET OE INT		Set overrun-error interrupt. Setting this bit enables the SCI module to generate an interrupt when an overrun error occurs.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.
24	SET PE INT		Set parity interrupt. Setting this bit enables the SCI module to generate an interrupt when a parity error occurs.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.
23-19	Reserved	0	Read returns 0. Writes have no effect.
18	SET RX DMA ALL		Set receive DMA all. This bit determines if a separate interrupt is generated for the address frames sent in multiprocessor communications. When this bit is 0, RX interrupt requests are generated for address frames and DMA requests are generated for data frames. When this bit is 1, RX DMA requests are generated for both address and data frames.
		0	*Read:* The DMA request is disabled for address frames (the receive interrupt request is enabled for address frames).
			Write: Writing a 0 to this bit has no effect.
		1	*Read and write:* The DMA request is enabled for address and data frames
17	SET RX DMA		Set receiver DMA. To enable receiver DMA requests, this bit must be set. If it is cleared, interrupt requests are generated depending on bit SCISETINT.
		0	*Read:* The DMA request is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read and write:* The DMA request is enabled for address and data frames

Table 27-6. SCI Set Interrupt Register (SCISETINT) Field Descriptions (continued)

Bit	Field	Value	Description
16	SET TX DMA		Set transmit DMA. To enable DMA requests for the transmitter, this bit must be set. If it is cleared, interrupt requests are generated depending on SET TX INT bit (SCISETINT).
		0	*Read:* Transmit DMA request is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read and write:* Transmit DMA request is enabled.
15-10	Reserved	0	Read returns 0. Writes have no effect.
9	SET RX INT		Receiver interrupt enable. Setting this bit enables the SCI to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.
8	SET TX INT		Set transmitter interrupt. Setting this bit enables the SCI to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.
7-2	Reserved	0	Read returns 0. Writes have no effect.
1	SET WAKEUP INT		Set wakeup interrupt. Setting this bit enables the SCI to generate a wakeup interrupt and thereby exit lowpower mode. If enabled, the wakeup interrupt is asserted when local lowpower mode is requested while the receiver is busy or if a low level is detected on the SCIRX pin during lowpower mode.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.
0	SET BRKDT INT		Set breakdetect interrupt. Setting this bit enables the SCI to generate an error interrupt if a break condition is detected on the SCIRX pin.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read or write:* The interrupt is enabled.

27.7.4 SCI Clear Interrupt Register (SCICLEARINT)

Figure 27-11 and Table 27-7 illustrate this register. SCICLEARINT register is used to clear the selected enabled interrupts with out accessing SCISETINT register.

Figure 27-11. SCI Clear Interrupt Register (SCICLEARINT) [offset = 10h]

31	27	26	25	24
Reserved		CLR FE INT	CLR OE INT	CLR PE INT
R-0		R/W-0	R/W-0	R/W-0
23	19	18	17	16
Reserved		CLR RX DMA ALL	CLR RX DMA	CLR TX DMA
R-0		R/WC-0	R/W-0	R/W-0
15		10	9	8
Reserved			CLR RX INT	CLR TX INT
R-0			R/W-0	R/W-0
7		2	1	0
Reserved			CLRWAKEUPINT	CLR BRKDT INT
R-0			R/W-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; WC = Write in sci-compatible mode only; *-n* = value after reset

Table 27-7. SCI Clear Interrupt Register (SCICLEARINT) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Read returns 0. Writes have no effect.
26	CLR FE INT		Clear framing-error interrupt. This bit disables the framing-error interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.
25	CLR CE INT		Clear overrun-error interrupt. This bit disables the SCI overrun error interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.
24	CLR PE INT		Clear parity interrupt. This bit disables the parity error interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.
23-19	Reserved	0	Read returns 0. Writes have no effect.
18	CLR RX DMA ALL		Clear receive DMA all. This bit clears the receive DMA request for address frames when set. Only receive data frames generate a DMA request.
		0	*Read:* Receive DMA request for address frames is disabled; Instead, RX interrupt requests are enabled for address frames. Receive DMA requests are still enabled for data frames.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The receive DMA request for address and data frames is enabled.
			Write: The receive DMA request for address and data frames is disabled.
17	CLR RX DMA		Clear receive DMA request. This bit disables the receive DMA request when set.
		0	*Read:* The DMA request is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The receive DMA request is enabled.
			Write: The receive DMA request for is disabled.

Table 27-7. SCI Clear Interrupt Register (SCICLEARINT) Field Descriptions (continued)

Bit	Field	Value	Description
16	CLR TX DMA		Clear transmit DMA request. This bit disables the transmit DMA request when set.
		0	*Read:* Transmit DMA request is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The transmit DMA request is enabled.
			Write: The transmit DMA request for is disabled.
15-10	Reserved	0	Read returns 0. Writes have no effect.
9	CLR RX INT		Clear receiver interrupt. This bit disables the receiver interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.
8	CLR TX INT		Clear transmitter interrupt. This bit disables the transmitter interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.
7-2	Reserved	0	Read returns 0. Writes have no effect.
1	CLR WAKEUP INT		Clear wakeup interrupt. This bit disables the wakeup interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.
0	CLR BRKDT INT		Clear breakdetect interrupt. This bit disables the break-detect interrupt when set.
		0	*Read:* The interrupt is disabled.
			Write: Writing a 0 to this bit has no effect.
		1	*Read:* The interrupt is enabled.
			Write: The interrupt is disabled.