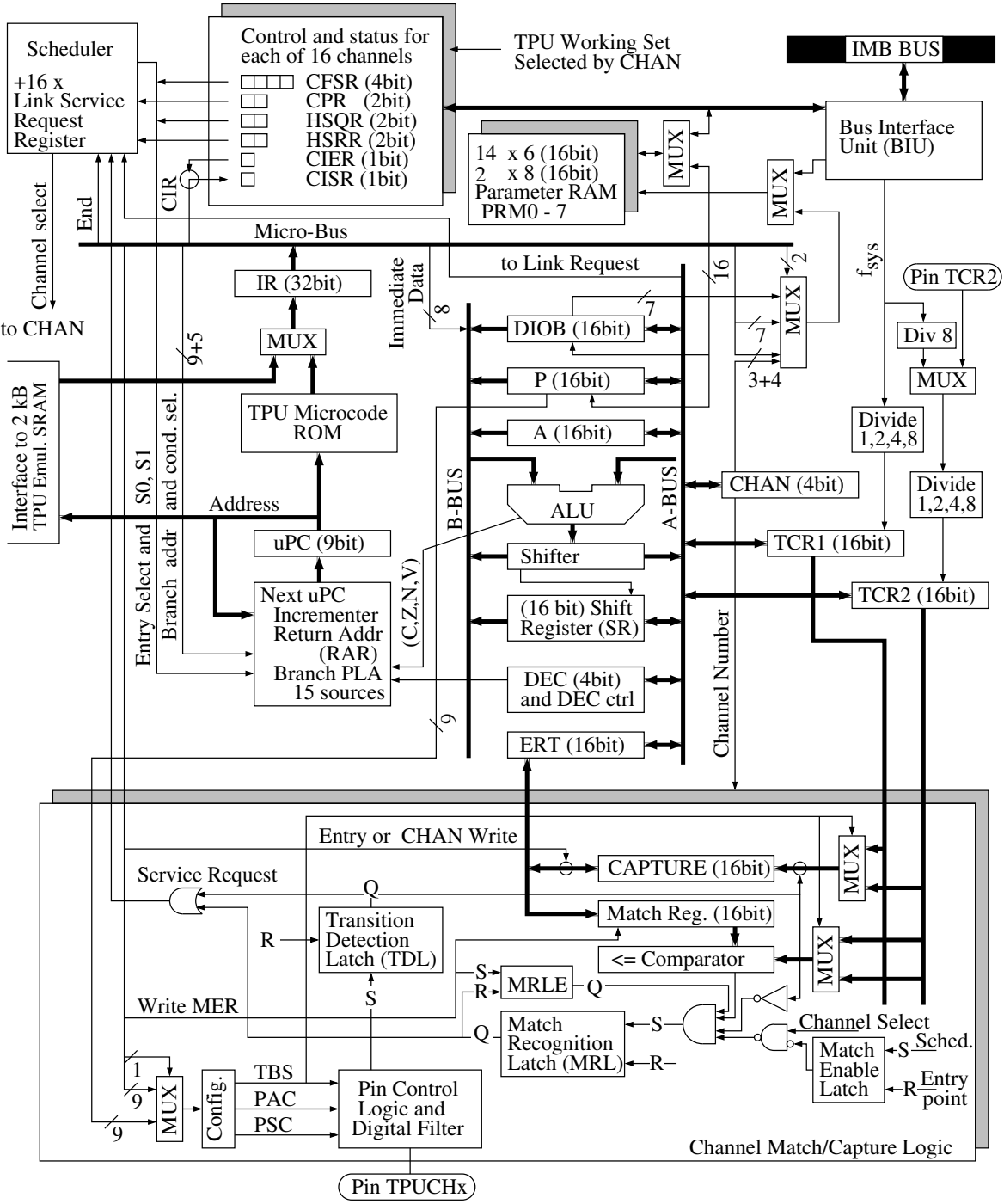
Scheduler
+16 x
Link Service
Request
Register
Control and status for
each of 16 channels
CFSR (4bit)
CPR (2bit)
HSQR (2bit)
HSRR (2bit)
CIER (1bit)
CISR (1bit)
TPU Working Set
Selected by CHAN
IMB BUS
Bus Interface
Unit (BIU)
14 x 6 (16bit)
2 x 8 (16bit)
Parameter RAM
PRM0 - 7
MUX
MUX
Channel select
End
CIR
Micro-Bus
to Link Request
16
2
f_{sys}
Pin TCR2
IR (32bit)
Immediate
Data
8
DIOB (16bit)
7
7
MUX
3+4
Div 8
MUX
to CHAN
MUX
9+5
P (16bit)
Interface to 2 kB
TPU Emul. SRAM
TPU Microcode
ROM
A (16bit)
Divide
1,2,4,8
S0, S1
and cond. sel.
B-BUS
A-BUS
CHAN (4bit)
Divide
1,2,4,8
Address
ALU
uPC (9bit)
Shifter
TCR1 (16bit)
Entry Select and
Branch addr
(C,Z,N,V)
Next uPC
Incrementer
Return Addr
(RAR)
Branch PLA
15 sources
(16 bit) Shift
Register (SR)
TCR2 (16bit)
Channel Number
DEC (4bit)
and DEC ctrl
9
ERT (16bit)
Entry or CHAN Write
CAPTURE (16bit)
MUX
Service Request
Q
Match Reg. (16bit)
Transition
Detection
Latch (TDL)
R
<= Comparator
MUX
S
R
MRLE
Q
Write MER
S
Q
Match
Recognition
Latch (MRL)
S
R
Channel Select
Match
Enable
Latch
S
Sched.
R
Entry
point
1
9
9
MUX
Config.
TBS
PAC
PSC
Pin Control
Logic and
Digital Filter
Channel Match/Capture Logic
Pin TPUCHx